ABSTRACT OF THE DISCLOSURE

A system and method are presented for an external host processor to distribute data to memory devices associated with multiple digital signal processors (DSPs) within an integrated circuit "system on a chip." A host processor interface in the multi-processor integrated circuit responds to commands from the host processor and provides access to the memory devices. A control register in the interface is directly accessible by the host processor, and is used to generate various control signals in response to host processor commands. A data control register in the interface has a field of write enable bits that directly control write accessibility of the memory devices – if a designated write enable bit within the data control register is set, the corresponding memory devices are write enabled. An extended address bit in the control register is used to select either instruction or data memory for write access. By using the write enable bits in the data control register together with the extended address bit in the control register, it is possible to simultaneously enable write access to any combination of the instruction memories or the data memories. This capability is useful when the multi-processor integrated circuit is first powered-up and must be initialized. With this invention, executable code may be loaded into the instruction memories of all the DSPs in a single operation. Similarly, data may be simultaneously placed in all the multi-processor integrated circuit data memories, rather than separately loading each data memory. As a result, multi-processor integrated circuit startup time may be significantly reduced.